Remarks

Reconsideration of this Application is respectfully requested.

Claims 1, 3-9, and 11-20 are pending in the application, with claims 1, 9, and 17 being the independent claims. No amendments have been made.

Based on the following remarks, Applicant respectfully requests that the Examiner reconsider all outstanding objections and rejections and that they be withdrawn.

Examiner Interview Summary

The Examiner is again thanked for his time during a telephonic interview with Applicant's representative Ed Yee on November 15, 2007. Applicant respectfully requests that the Examiner send an Interview Summary of the above-mentioned interview.

Rejections under 35 U.S.C. § 102

Claims 1, 3, 5, 6, 10, 11, 13, 14, and 17-20 were rejected under 35 U.S.C. § 102(b) as being allegedly anticipated by U.S. Patent No. 5,361,185 to Yu (Yu). Applicant respectfully traverses this rejection.

As claim 10 was previously cancelled and as the Examiner refers to claim 9 in his rejection, Applicant assumes that the Examiner intended that claims 1, 3, 5, 6, 9, 11, 13, 14, and 17-20 were rejected under 35 U.S.C. § 102(b) as being allegedly anticipated by Yu. Applicant respectfully traverses this rejection.

Claims 1, 9, and 17 recite features which distinguish over Yu. For example, claim 1 recites "wherein the ESD protection system is connected in series between the pad and the n-type transistor, and substantially eliminates ESD from flowing from the pad into the n-type transistor, and the size of the n-type transistor and the size of the ESD protection system collectively are less than the size of a single n-type transistor adapted to comply with both the operational requirement and the ESD requirement." Claim 9 recites "wherein the size of the n-type transistor and the size of the means for protecting the circuit collectively are less than the size of a single n-type transistor adapted to comply with both the operational requirement and the ESD requirement." Claim 17 recites "wherein the one of the NMOS transistor and the PMOS transistor is connected in series between the pad and the n-type transistor, and substantially eliminates ESD from flowing from the pad into the n-type transistor, and the size of the n-type transistor and the size of the one of the NMOS transistor and the PMOS transistor collectively are less than the size of a single n-type transistor adapted to comply with both the operational requirement and the ESD requirement."

The Examiner states in the Office Action that, regarding claims 1 and 9:

> Yu discloses a system (figure 1) comprises a circuit (Q3) comprising an n type, the n type transistor adapted to comply with an operational requirement, an ESD protection system (10) adapted to comply with an ESD requirement, and a pad (14), wherein the ESD protection system (10) is connected in series between the pad and the n type transistor and substantially eliminates ESD from flowing from the pad into the n type transistor...and the size of the n-type transistor (Q3, see col. 3, lines 55-57) and the size of the ESD protection system (see col. 4, lines 4-6) collectively are less than the size of single n type transistor (e.g. Q2 has a area 272, see col. 3 lines 44-48) adapted to comply with the operational and ESD

> requirements (the total sizes of Q3 and Q4 is less than the size of Q2).

(Office Action, pp. 2-3). The Examiner states regarding claim 17 that

> Yu discloses a system (figure 1) comprises a circuit (NMOS transistor Q3) comprising an n type, the n type transistor adapted to comply with an operational requirement, one of a NMOS, an a PMOS transistor (NMOS transistor Q4 of the ESD protection 10) adapted to comply with an ESD requirement, and a pad (pad 14), wherein the one of the NMOS transistor and the PMOS transistor is connected in series between the pad and the n type transistor and substantially eliminates ESD from flowing fronm the pad into the circuit...and the size of the n type transistor...and the one of NMOS transistor and the PMOS transistor (the size of NMOS transistor Q4...) collectively is less the size of a single n type transistor (the size of transistor Q2...) adapted to comply with the operational and ESD requirement.

(Office Action, pp. 3-4). Applicant respectfully disagrees with the Examiner's characterization of Yu.

Yu describes "[a] distributed VCC/VSS clamp structure (**10**) for preventing inadvertent damage to semiconductor integrated circuits caused by an electrostatic discharging event. (Yu, Abstract.) Yu further states, "[t]he clamp transistor is activated only when the ESD protection circuitry is unable to supply a primary discharging path." (Yu, col. 2, lines 50-54). Thus, Yu describes two ESD protection systems: a primary system and a secondary system.

Yu continues, "[t]he input or output pad **14** is coupled to an internal circuit **16** to be protected via an internal node A." (Yu, col. 3, lines 34-35). Yu describes an ESD structure that is "quite conventional and does not form a part of the present invention." (Yu, col. 3, lines 62-64). Yu states that this conventional ESD structure includes "a first N-channel MOS transistor **Q1** and a second N-channel MOS transistor **Q2**...The ESD

structure **12** further includes a third N-channel MOS transistor **Q3** having its drain connected to the internal node B and to the gates of the first and second MOS transistors **Q1** and **Q2**." (Yu, col. 3, lines 35-52; FIG. 1). Thus, Yu describes a primary ESD structure, labeled **12** in Figure 1, that is comprised of three N-channel MOS transistors Q1, Q2, and Q3. This ESD structure **12** is designed to protect internal circuit **16**. Thus, Q2 is not "adapted to comply with the operational **and** ESD requirement" as stated by the Examiner. (Office Action, p. 4) (emphasis added). Instead, Q2 is part of the primary ESD structure only. Further, in contrast to the Examiner's implication in the Office Action, Yu's internal circuit **16** is the circuit to be protected, and not Yu's Q3.

Therefore, Yu does not disclose or suggest "wherein...the size of the n-type transistor and the size of the ESD protection system collectively are less than the size of a single n-type transistor adapted to comply with both the operational requirement and the ESD requirement" as recited in claim 1, or "wherein the size of the n-type transistor and the size of the means for protecting the circuit collectively are less than the size of a single n-type transistor adapted to comply with both the operational requirement and the ESD requirement" as recited in claim 9, or "wherein...the size of the n-type transistor and the size of the one of the NMOS transistor and the PMOS transistor collectively are less than the size of a single n-type transistor adapted to comply with both the operational requirement and the ESD requirement" as recited in claim 17.

Yu states that the secondary ESD structure **10** of "the present invention is comprised of a fourth N-channel MOS transistor **Q4**...The gate of the transistor **Q4** is connected to the gates of the transistors **Q1** and **Q2** at the internal node B." (Yu, col. 3, line 65 to col. 4, line 3; FIG. 1). Thus, primary ESD structure **12** and secondary ESD

structure **10** are both designed to protect the internal circuit **16**. Thus, Q1, Q2, Q3, and Q4 are all present in Yu's protection circuit, which is comprised of both the primary ESD structure **12** and the secondary ESD structure **10**, as shown in Yu's figure 1. In addition, because Q1, Q2, Q3, and Q4 are ***all*** present in Yu's ESD protection circuit and because Q3 is not the circuit to be protected, the size of Q3 and Q4 relative to the size of Q2 is irrelevant, in contrast to the Examiner's statement in the Office Action.

Therefore, for this reason as well, Yu does not disclose or suggest "wherein...the size of the n-type transistor and the size of the ESD protection system collectively are less than the size of a single n-type transistor adapted to comply with both the operational requirement and the ESD requirement" as recited in claim 1, or "wherein the size of the n-type transistor and the size of the means for protecting the circuit collectively are less than the size of a single n-type transistor adapted to comply with both the operational requirement and the ESD requirement" as recited in claim 9, or "wherein...the size of the n-type transistor and the size of the one of the NMOS transistor and the PMOS transistor collectively are less than the size of a single n-type transistor adapted to comply with both the operational requirement and the ESD requirement" as recited in claim 17.

For at least these reasons, Yu does not anticipate claims 1, 9, and 17. For at least these reasons, claims 1, 9, and 17 are patentable over Yu.

Claims 3, 5, 6, and 18 depend from claim 1. For at least these reasons, and further in view of their own features, dependent claims 3, 5, 6, and 18 are patentable over Yu.

Claims 11, 13, 14, and 19 depend from claim 9. For at least these reasons, and further in view of their own features, dependent claims 11, 13, 14, and 19 are patentable over Yu.

Claim 20 depends from claim 17. For at least these reasons, and further in view of its own features, dependent claim 20 is patentable over Yu.

Reconsideration and withdrawal of the rejections are respectfully requested.

Rejections under 35 U.S.C. § 103

Claims 4 and 12

Claims 4 and 12 were rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Yu in view of U.S. Patent No. 5,499,152 to Tamakoshi (Tamakoshi). Applicant respectfully traverses this rejection.

For a rejection to be legally adequate under 35 U.S.C. § 103, every claim limitation must similarly be taught by, or be obvious to a person of ordinary skill in the art from, the combination of the references. See *Orthopedic Equipment, Inc. v. United States*, 702 F.2d 1005, 1013 (Fed. Cir. 1983).

As discussed above, Yu does not teach or suggest all the features of claims 1 and 9.

The Examiner argues that in Tamakoshi "an ESD protection system (figure 4) comprises a resistor (the resistor R)." (Office Action, p. 5). Tamakoshi does not teach or suggest the above-recited distinguishing features of claims 1 and 9. Thus, Tamakoshi does not overcome the deficiencies of Yu relative to claims 1 and 9, described above.

Therefore, the applied references cannot be used to establish a prima facie case of obviousness with respect to claims 1 and 9.

Claim 4 depends from claim 1. Thus, at least based on its dependency to claim 1, and further in view of its own features, claim 4 is patentable over the applied references.

Claim 12 depends from claim 9. Thus, at least based on its dependency to claim 9, and further in view of its own features, claim 12 is patentable over the applied references.

Reconsideration and withdrawal of the rejection is respectfully requested.

Claims 7, 8, 15, and 16

Claims 7, 8, 15, and 16 were rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Yu in view of U.S. Patent No. 3,746,946 to Clark (Clark). Applicant respectfully traverses this rejection.

As discussed above, Yu does not teach or suggest all the features of claims 1 and 9.

The Examiner states in the Office Action: "Yu does not disclose the ESD protection system comprises a PMOS transistor as claimed." (Office Action, p. 5). The Examiner argues that Clark teaches "a PMOS transistor based on such the design constraints because this is a known type protection as disclosed by Clark." (Office Action, p. 5).

Clark does not teach or suggest the above-recited distinguishing features of claims 1 and 9. Thus, Clark does not overcome the deficiencies of Yu relative to claims 1 and 9, described above. Therefore, the applied references cannot be used to establish a prima facie case of obviousness with respect to claims 1 and 9.

Claims 7 and 8 depend from claim 1. Thus, at least based on their dependency to claim 1, and further in view of their own features, claims 7 and 8 are patentable over the applied references.

Claims 15 and 16 depend from claim 9. Thus, at least based on their dependency to claim 9, and further in view of their own features, claims 15 and 16 are patentable over the applied references.

Reconsideration and withdrawal of the rejection is respectfully requested.

Conclusion

All of the stated grounds of objection and rejection have been properly traversed, accommodated, or rendered moot. Applicant therefore respectfully requests that the Examiner reconsider all presently outstanding objections and rejections and that they be withdrawn. Applicant believes that a full and complete reply has been made to the outstanding Office Action and, as such, the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Reply is respectfully requested.

Respectfully submitted,

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